5,604,741 issued February 18, 1997, the disclosures of which are incorporated fully herein by reference.

On page 3, kindly delete lines 3-45 and substitute the following summary of the invention:

A first apparatus embodiment of the invention is useful in an apparatus that is adapted to be coupled to at least one pair of twisted wires that carry a plurality of analog levels defining information signals. In such an environment, an analog to digital converter is arranged to convert the plurality of analog levels to corresponding digital information signals at a particular rate. A timing recovery circuit is arranged to regulate the particular rate at which the analog to digital converter converts the plurality of analog levels to the corresponding digital information signals. A digital adaptive equalizer is arranged to receive the digital information signals and is arranged to identify one of the digital information signals with a level corresponding most closely to one of the plurality of analog levels defining information signals.

A second apparatus embodiment of the invention is useful in an apparatus that is adapted to be coupled to at least one pair of twisted wires that carry a plurality of analog levels defining information signals. In such an environment, a clock is arranged to generate clock signals having a phase, and an analog to digital converter is arranged to convert the plurality of analog levels to corresponding information digital signals in response to the clock signals. A timing recovery circuit is arranged to shift the phase of the clock signals so that time at which the analog to digital converter samples the analog levels is adjusted. A digital adaptive equalizer is arranged to receive the digital information signals and to identify one of the digital information signals with a level

corresponding most closely to one of the plurality of analog levels defining information signals.

A third apparatus embodiment of the invention is useful in an apparatus that is adapted to be coupled to at least one pair of twisted wires that carry a multi-level signal. In such an environment, an analog to digital converter digitally converts the multi-level signal at a particular rate. A timing recovery circuit regulates the particular rate at which the analog to digital converter converts the multi-level signal in accordance with a product of a plurality of peak signal samples. A digital adaptive equalizer receives the digitally converted multi-level signal and identifies one of a plurality of levels.

A fourth apparatus embodiment of the invention is useful in an apparatus that is adapted to be coupled to at least one pair of twisted wires that carry a multi-level signal transmitted at a transmission rate of at least 25 megasymbols per second. In such an environment, an analog to digital converter that is responsive to the multi-level signal transmitted at the transmission rate of at least 25 megasymbols per second is provided. A clock recovery circuit is coupled to the analog to digital converter that regulates the particular rate in accordance with a product of a plurality of peak signal samples. A digital adaptive equalizer is coupled to the analog to digital converter.

A fifth apparatus embodiment of the invention is useful in an apparatus that is adapted to be coupled to at least one pair of twisted wires that carry a multi-level signal. In such an environment an analog to digital converter operates at a particular rate. A clock recovery circuit coupled to the analog to digital converter regulates the particular rate in accordance with a product of a plurality of peak signal samples, and a digital adaptive equalizer is coupled to the analog to digital converter.

A sixth apparatus embodiment of the invention is useful in an apparatus adapted to be coupled to at least a twisted first wire pair enabling receipt of at least first, second and third discrete analog signal levels with different amplitudes representing information, a twisted second wire pair enabling receipt of at least fourth, fifth and sixth discrete analog signal levels with different amplitudes representing information and a twisted third wire pair enabling receipt of at least seventh, eighth and ninth discrete analog signal levels with different amplitudes representing information. The analog signal levels are received one discrete signal level at a time. In such an environment, the discrete analog signal levels may be processed by providing apparatus comprising an analog to digital converter arranged to convert the first discrete analog signal level to a corresponding digital first information signal, to convert the second discrete analog signal level to a corresponding digital second information signal, to convert the third discrete analog signal level to a corresponding digital third information signal, to convert the fourth analog signal level to a corresponding digital fourth information signal, to convert the fifth discrete analog signal level to a corresponding digital fifth information signal, to convert the sixth discrete analog signal level to a corresponding digital sixth information signal, to convert the seventh discrete analog signal level to a corresponding digital seventh information signal, to convert the eighth discrete analog signal level to a corresponding digital eighth information signal and to convert the ninth discrete analog signal level to a corresponding digital ninth information signal. Circuitry is arranged to individually identify each of the first, second, third, fourth, fifth, sixth, seventh, eighth and ninth discrete analog signal levels. The circuitry also shifts in time the first information signal relative to the first discrete analog signal level, shifts in time

the second information signal relative to the second discrete analog signal level, shifts in time the third information signal relative to the third discrete analog signal level, shifts in time the fourth information signal relative to the fourth discrete analog signal level, shifts in time the fifth information signal relative to the fifth discrete analog signal level, shifts in time the sixth information signal relative to the sixth discrete analog signal level, shifts in time the seventh information signal relative to the seventh discrete analog signal level, shifts in time the eighth information signal relative to the eighth discrete analog signal level and shifts in time the ninth information signal relative to the ninth discrete analog signal level.

A first method embodiment of the invention is useful for recovering a plurality of analog levels defining information signals transmitted on at least one pair of twisted wires by converting the plurality of analog levels defining information signals to corresponding digital information signals at a particular rate, regulating the particular rate of conversion and identifying one of the digital information signals with a level corresponding most closely to one of the plurality of analog levels defining information signals.

A second method embodiment of the invention is useful for recovering a plurality of analog levels defining information signals transmitted on at least one pair of twisted wires by generating clock signals having a phase, converting the plurality of analog levels to corresponding digital information signals in response to the clock signals, shifting the phase of the clock signals so that time at which the timing recovery circuit samples the analog levels is adjusted and receiving the corresponding digital information signals and identifying one of the digital information signals with a level

corresponding most closely to one of the plurality of analog levels defining information signals.

A third method embodiment of the invention is useful for recovering a multi-level signal transmitted on at least one pair of twisted wires by converting the multi-level signal to a digital signal at a particular rate, regulating the particular rate of conversion in accordance with a product of a plurality of peak signal samples, equalizing the digital signal and identifying one of a plurality of levels based on the digital signal.

A fourth method embodiment of the invention is useful in apparatus adapted to be coupled to at least a twisted first wire pair enabling receipt of at least first, second and third discrete analog signal levels with different amplitudes representing information, a twisted second wire pair enabling receipt of at least fourth, fifth and sixth discrete analog signal levels with different amplitudes representing information and a twisted third wire pair enabling receipt of at least seventh, eighth and ninth discrete analog signal levels with different amplitudes representing information. The analog signal levels are received one discrete signal level at a time. In such an environment, the received discrete analog signal levels may be processed by implementing a method comprising:

converting the first discrete analog signal level to a corresponding digital first information signal;

converting the second discrete analog signal level to a corresponding digital second information signal;

converting the third discrete analog signal level to a corresponding digital third information signal;

converting the fourth discrete analog signal level to a corresponding digital fourth information signal;

converting the fifth discrete analog signal level to a corresponding digital fifth information signal;

converting the sixth discrete analog signal level to a corresponding digital sixth information signal;

converting the seventh discrete analog signal level to a corresponding digital seventh information signal;

converting the eighth discrete analog signal level to a corresponding digital eighth information signal;

converting the ninth discrete analog signal level to a corresponding digital ninth information signal;

individually identifying each of the first, second, third, fourth, fifth, sixth, seventh, eighth and ninth discrete analog signal levels;

shifting in time the first information signal relative to the first discrete analog signal level;

shifting in time the second information signal relative to the second discrete analog signal level;

shifting in time the third information signal relative to the third discrete analog signal level;

shifting in time the fourth information signal relative to the fourth discrete analog signal level;

shifting in time the fifth information signal relative to the fifth discrete analog signal level;

shifting in time the sixth information signal relative to the sixth discrete analog signal level;

shifting in time the seventh information signal relative to the seventh discrete analog signal level;

shifting in time the eighth information signal relative to the eighth discrete analog signal level; and

shifting in time the ninth information signal relative to the ninth discrete analog signal level.

In The Claims:

Kindly cancel claims 152-162.

Kindly amend claims 145, 150, 151, 163, 164 and 166 as follows:

145. (Amended) An apparatus that is adapted to be coupled to at least one pair of twisted wires that carry a plurality of analog levels defining information signals comprising:

an analog to digital converter arranged to convert the plurality of analog levels to corresponding digital information signals at a particular rate;

a timing recovery circuit arranged to regulate the particular rate at which said analog to digital converter converts the plurality of analog levels to the corresponding digital information signals; and